Distributed Clock Useful Skew to Reduce Peak Current

The Flexible ASIC Leader
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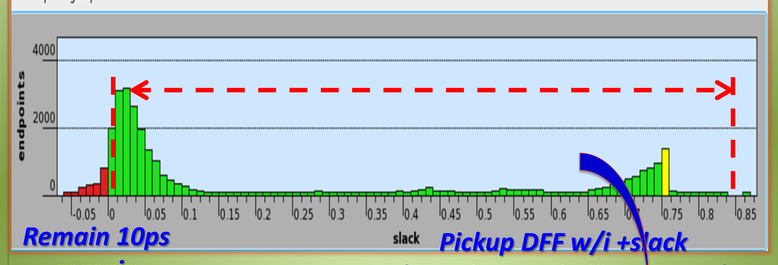
Methodology : Flatten Mode

Scenario	Mode	Corner	Path Group	Analysis	Endpoints	NVE	WNS
FUNC_cworst_T_ssg0p81v0c_SETUP	FUNC	cworst_T_ssg0p81v0c_SETUP	RegOut	setup	3236		50
FUNC_cworst_T_ssg0p81v0c_SETUP	FUNC	cworst_T_ssg0p81v0c_SETUP	reg2reg	setup	32194		1865
FUNC_cworst_T_ssg0p81v0c_SETUP	FUNC	cworst_T_ssg0p81v0c_SETUP	to_sram	setup	2688		23

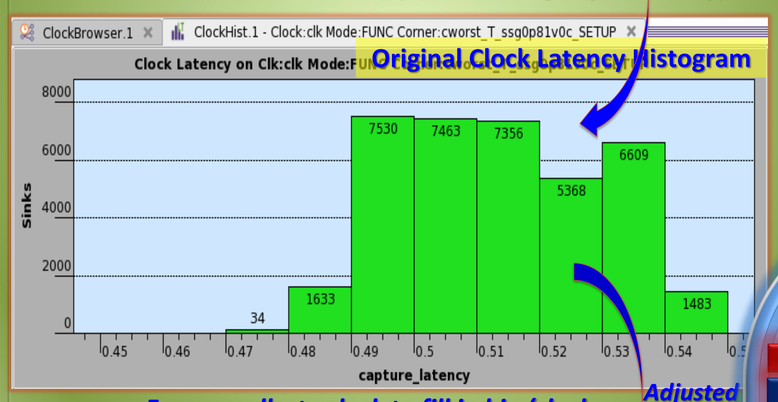
24 endpoint groups

PreCTS Setup Histogram



Remain 10ps margin

Pickup DFF w/i +slack (remain margin if necessary)

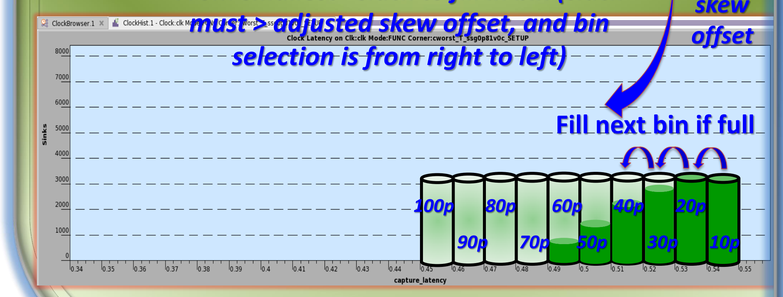


Original Clock Latency Histogram

From smallest +slack to fill in bin (slack must > adjusted skew offset, and bin selection is from right to left)

Adjusted skew offset

Fill next bin if full



Motivation & Objective

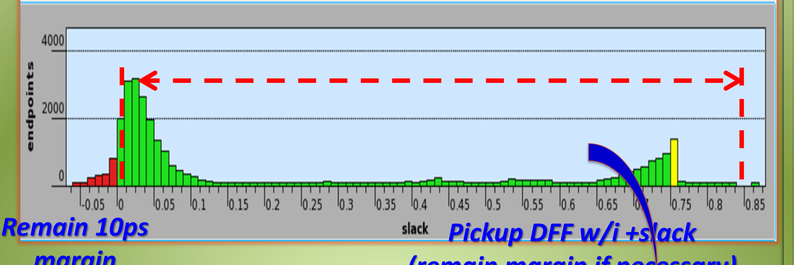
- For synchronous digital designs, the huge peak current are induced by concurrently switching of clock buffer tree, simultaneous triggering sequential logic and the signal propagation through the sequential logic to the large amount of combination logic.
- Traditional clock tree synthesis approach, zero clock skew is first priority to gain max frequency, and apply useful skew if frequency still can't reach. But about the useful skew of sequential logic with positive slack, there is no particular application.
- We are proposing a methodology of utilizing useful skew of sequential logic with positive slack. Applying clock latency constraint for CTS to distribute the simultaneous switching of sequential logic.

Methodology : Two Cluster Mode

Scenario	Mode	Corner	Path Group	Analysis	Endpoints	NVE	WNS
FUNC_cworst_T_ssg0p81v0c_SETUP	FUNC	cworst_T_ssg0p81v0c_SETUP	RegOut	setup	3236		50
FUNC_cworst_T_ssg0p81v0c_SETUP	FUNC	cworst_T_ssg0p81v0c_SETUP	reg2reg	setup	32194		1865
FUNC_cworst_T_ssg0p81v0c_SETUP	FUNC	cworst_T_ssg0p81v0c_SETUP	to_sram	setup	2688		23

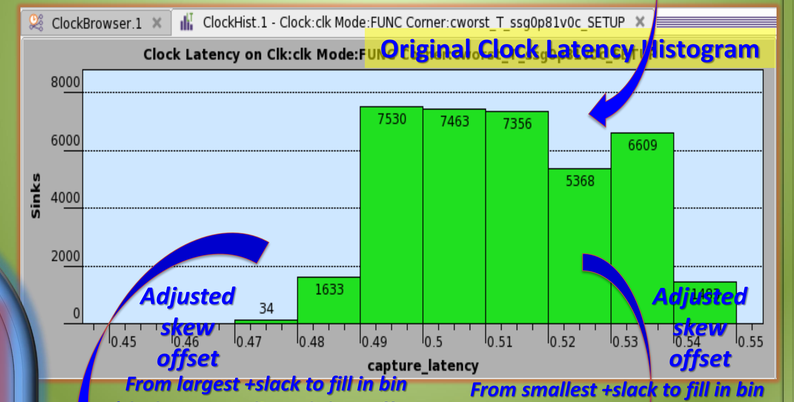
24 endpoint groups

PreCTS Setup Histogram



Remain 10ps margin

Pickup DFF w/i +slack (remain margin if necessary)



Original Clock Latency Histogram

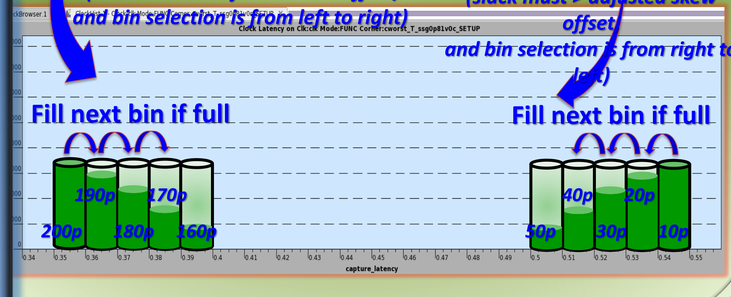
Adjusted skew offset

From largest +slack to fill in bin (slack must > adjusted skew offset, and bin selection is from left to right)

Adjusted skew offset

From smallest +slack to fill in bin (slack must > adjusted skew offset, and bin selection is from right to left)

Fill next bin if full

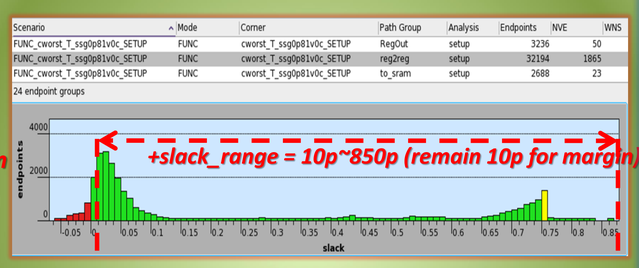


Fill next bin if full

PreCTS Clock Latency Analysis

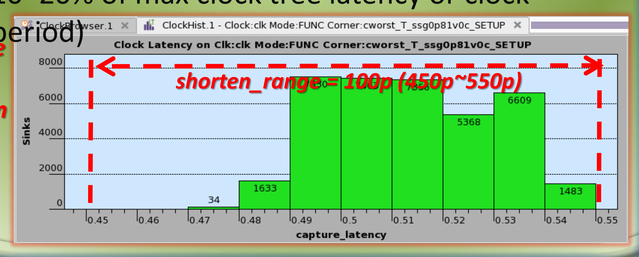
- On PreCTS stage, specify parameters for skew adjustment
  - ➢ View timing slack histogram of the worst scenario, decide the +slack range for adjustment

Timing slack histogram



  - ➢ View the trial clock tree latency histogram, set the shorten range of clock tree latency (suggest 10~20% of max clock tree latency or clock period)

Clock tree latency histogram



: Original Tasks
: Additional Tasks

Placement

Specify mode & params

Distribute Useful Skew

CTS

Adjust mode & params

PostCTS Opt

Not accept

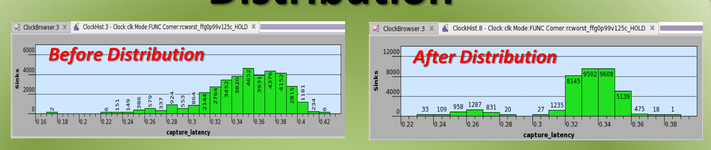
Check QoR

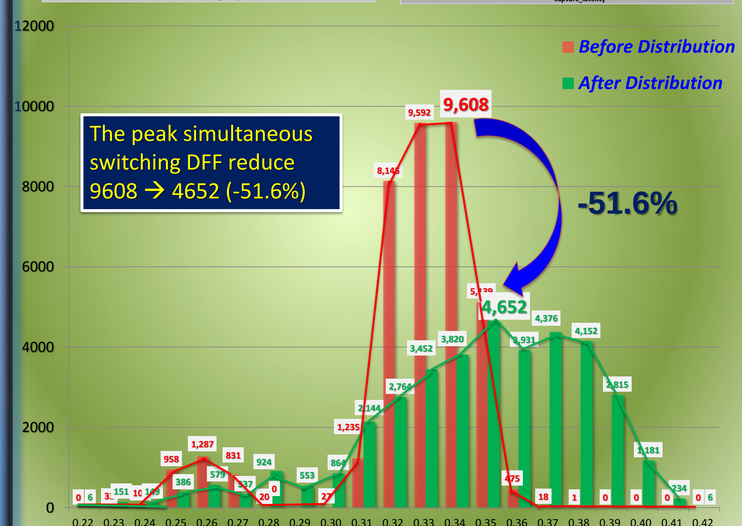
Accept

Route

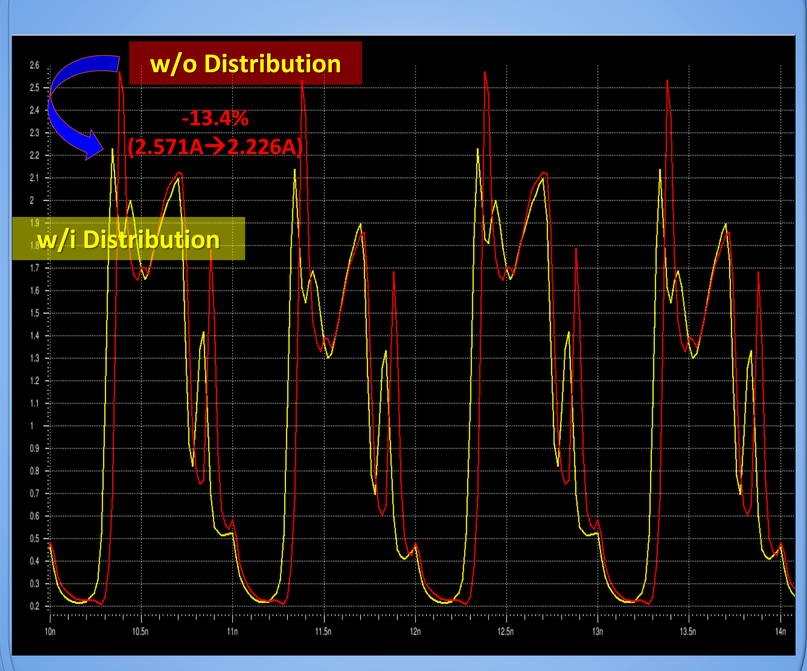
- ◆ Check endpoint w/i +slack & specify skew offset within +slack evenly
- ◆ Generate
  - set_clock_latency.tcl (for check timing)
  - set_clock_balance_points.tcl (for CTS)
- ◆ Source set_clock_latency.tcl to make sure there is no timing impact on PreCTS stage
- ◆ Source set_clock_balance_points.tcl before CTS to constraint balancing value
- ◆ Review the histogram of clock tree latency distribution
- ◆ Run RedHawk or ICC2-AF to make sure the ratio of peak current is acceptable (option)
- ◆ Check any PPA impact & accept it if minor

PostCTS Clock Latency Distribution





PostRoute Current Waveform



Conclusions

- The reduction of simultaneous switching of sequential logic is related to peak current positively. But why the reduction ratio is not direct proportion?
  - ➢ The power of sequential logic is only 6% of total power (comb. is 39.7%, clock network 38.5%, memory 15.7%), our method is only to distribute sequential logic & memory part.
- The effect of Power/Leakage reduction at PostRoute stage will be less caused by timing margin has already been applied for clock tree latency distribution.
- Distribution clock tree latency is focus on adjustment skew of positive slack, the CCD is focus on negative slack, so both methods can apply together w/o concern.

Future Works

- Support MCMM modes

Evaluation Results

	Original Flow	New Flow (Peak Current Reduction)	Difference (Org/New)
Area (um²)	374392	379698	+1.4%
Timing (WNS/TNS/NVE)	Setup (-0.16/-18.5/3059) Hold (-0.12/-2.25/363)	Setup (-0.14/-39.4/4157) Hold (-0.13/-9.9/696)	Setup (+0.02/-20.9/1098) Hold (-0.01/-7.65/333)
Total Power (Watt)	0.3826	0.3912	+2.2%
IR (SIR / DIR)	1.35% / 6.74%	1.37% / 6.34%	+0.02% / -0.4%
Peak Current (A)	2.571	2.226	**-13.4%**
Flow Complexity	NA	3 APR commands & 2 check points (PostCTS & PostRoute)	